UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,251	02/09/2005	Dag Behammer	BEHAMMER 6 PCT	4600

25889 7590 12/29/2005

WILLIAM COLLARD
COLLARD & ROE, P.C.
1077 NORTHERN BOULEVARD
ROSLYN, NY 11576

EXAMINER	
LEE, CHEUNG	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,251	BEHAMMER, DAG	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-09-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ETAILED ACTION

Notice to Applicant

1. Applicant's Preliminary Amendment filed on February 9, 2005 has been entered and made of record.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on February 9, 2005 was filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claims 1-11 are objected to because of the following informalities: in claim 1, structural language is used instead of method language, e.g., "the wafer is attached" should be "attaching the wafer" in method claims. Appropriate correction is required.

Claims 2-11 depend from claim 1, so they are objected for the same reason.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Claim 1 recites the limitation "the intermediate layer" in step d), lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-11 depend from claim 1, so they are rejected for the same reason.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al. (US Pat. 5919713; hereinafter "Ishii").

6. With respect to claim 1, referring to figures 1-3, Ishii discloses method for the production of individual monolithically integrated semiconductor circuits 101, 102, 103, 104, which have a component structure (see figure 2A, items 103, 104) on the front face (opposite side of 11a) of a substrate 1 that has been reduced in thickness, and a metallized 22 substrate back face 11a, as well as electrical connections 21 between the metallic substrate back face and conductive surfaces (bottom surfaces of 13) on the front face, by way of passage holes 13a through the substrate, from a wafer (fig. 1, item 1), the examiner takes the position that a semiconductor substrate is normally at least a portion of a semiconductor wafer, containing a plurality of separate component structures 101, 102, 103, 104, wherein a) the wafer is attached to a rigid carrier 19 after completion of the front face component structures, with the front face surface (col. 5, lines 54-67), by means of an attachment layer 18, over its entire area (see fig. 2B), b)

the substrate is reduced to the desired thickness (col. 6, lines 1-10), c) the passage holes 13a through the substrate are produced up to the conductive surfaces on the front face (see fig. 2C), d) the separating trenches 11 between the monolithic semiconductor circuits 103, 104 are produced up to or into an intermediate layer 16, e) the back face metallization 22, including the electrical connections 21 through the passage holes, is produced, f) the semiconductor circuits are individually released from the rigid carrier (col. 6, lines 39-49; col. 7, lines 10-27) and individually processed further (col. 7, lines 10-27).

7. With respect to claim 2, Ishii discloses wherein an adhesive material (col. 6, lines 1-10) is used for the attachment layer. Ishii discloses a wax layer 18 which uses to attach the semiconductor substrate and the support substrate together, the examiner considers the wax layer to be the adhesive material.

8. With respect to claim 5, Ishii discloses wherein the substrate is reduced in thickness to a thickness of less than 100 μm (col. 6, lines 1-10).

9. With respect to claim 6, Ishii discloses wherein the separating trenches are produced by means of a photolithographic etching process (col. 6, lines 11-23).

10. With respect to claim 7, Ishii discloses wherein a protective layer 17 is applied on the front face of the wafer (see fig. 2A).

11. With respect to claim 8, Ishii does not disclose expressly wherein a lateral under-etching of the substrate is produced in the front face protective layer of the wafer. However, Ishii discloses a wet etching process with aqueous solution to etch the dicing regions and through-holes (col. 6, lines 11-23). Because of the isotropic nature the aqueous solution laterally under-etch of the protective layer.

12. With respect to claim 9, Ishii discloses wherein the deposition of the back face metallization is performed after production of the separating trenches (col. 6, lines 11-45).

13. With respect to claim 10, Ishii discloses wherein a common photolithographic mask 20 is used for the production of the passage holes and the separating trenches.

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Nakanishi et al. (US Pub. 2001/0005043; hereinafter "Nakanishi").

Ishii does not disclose expressly wherein an adhesive material having a lower adhesion to the front face surface of the wafer when a higher temperature is used.

Referring to figures 1(a)-1(c), Nakanishi discloses adhesive layers 33, 36, e.g., wax, for bonding a semiconductor wafer and support substrates (page 4, paragraphs 63-64). The adhesive layer 33 is heated to about 110°C to separate two substrates 32, 34 (page 4, paragraphs 66-67; fig. 1(b)). This means that the wax adhesion gets lowered with heat.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the adhesive layer for bonding, as taught by Nakanishi.

The motivation for doing so would have been to obtain high yields separating two substrates without any external force, which may cause cracking, in a short time (Nakanishi, page 4, paragraph 67).

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Sugino et al. (US Pub. 2002/0055238; hereinafter "Sugino").

Ishii does not disclose expressly wherein the individual release of the semiconductor circuits from the carrier is performed mechanically, overcoming the adhesion force of the attachment material to the front face of the wafer.

Referring to figure 7, Sugino discloses a die which is picked up from a base 31 of the dicing/die bond sheet 30 (page 5, paragraph 97; see fig. 7) overcoming adhesion force, because the adhesive strength of an adhesive layer 32 is lowered by an exposure to energy radiation (page 5, paragraph 98).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the pickup step, as taught by Sugino.

The motivation for doing so would have been to keep chips aligned while detaching chips from the base thereby enable improving a pickup efficiency.

16. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Mignardi et al. (US Pat. 5597767; hereinafter "Mignardi").

Ishii does not disclose expressly wherein an electrical function test of the semiconductor circuits is performed after separation.

Referring to figures 1-3, Mignardi discloses a testing step of dies (col. 5, lines 32-39; step 24). Also, it would have been obvious to test each die right before the packaging (col. 4, lines 26-39).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to test each semiconductor circuit, as taught by Mignardi.

The motivation for doing so would have been to help picking and shipping only good quality semiconductor circuits to customers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

December 21, 2005

HA NGUYEN
PRIMARY EXAMINER